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10/717,042	11/18/2003	William A. Wilkie	X-1455 US	7433

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EXAMINER	
TU, CHRISTINE TRINH LE	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/717,042	WILKIE ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-35* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-35* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/18/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Objections

1. Claims 20, 29 and 35 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form.

Claim 20:

The limitation in this claim is similar to the phrase "said multi-stage clocked storage device comprises ... said clocked storage stages" (at lines 3-4 of claim 19).

Claim 29:

At lines 2-4, the limitation "producing a plurality of sum ... comprises producing said first sum and producing said second sum" in this claim is similar to the limitation "producing a first sum... producing a second sum..." (at lines 2-7 of claim 24).

At lines 5-6, the limitation of "said producing said selected sum further comprises selecting a selected one of said sums" is similar to the limitation "producing a selected sum by selecting a one of said first sum and said second sum" (at lines 8-9 of claim 24).

Claim 35:

At lines 2-5, the limitation "means for producing a plurality of sum ... comprises said means for producing said first sum and said means for producing said second sum"

in this claim is similar to the limitation "producing a first sum... producing a second sum..." (at lines 2-8 of claim 30).

At lines 6-8, the limitation of "said means for producing said selected sum further comprises means for selecting one of said sums" is similar to the limitation "means for producing a selected sum comprising means for selecting a one of said first sum and said second sum" (at lines 9-11 of claim 30).

Claim Rejections - 35 USC § 112

2. Claims 1-35 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1-6 and 10-15:

Throughout all claims, due to lack of performance for each element in the claims, it is not clear how one element is being interrelated with another (or the other) element(s) besides they are just coupling to each other.

In other words, it is not clear what performance each element has in order to carryout the invention (beside such elements are just coupling to each other).

Applicant is request to reformat the claim to include an "ing" ending word for each structure element after a preposition "for" (i.e. a compare unit … for comparing …; each of said adder unit for adding …; a selection unit for selecting …).

Claim 3:

Due to so many different adder units have been previously recited, it is not clear whether the term "said adder unit" (at line 3) refers back to the "adder unit" (as being recited at line 2 of claim 2), or refers back to one of the "plurality of adder units" (as being recited at line 5 of claim 1).

Claim 4:

Due to so many different adder units have been previously recited, it is not clear whether the term "said adder units" (at line 2) refers back to the "plurality of adder units" (as being recited at line 5 of claim 1), or refers back to all of the adder units (as being recited at line 5 of claim 1 and at line 2 of claim 2).

Claims 5 and 6:

Due to so many different adder units have been previously recited, it is not clear whether the term "one of said adder units" (at line 3) refers back to one of the plurality of adder units (as being recited at line 5 of claim 1), or refers back to the adder unit (as being recited at line 2 of claim 2).

Claim 5:

Due to the fact that so many different adder units have been previously recited, it is not clear whether the term "said adder unit" (at line 4) refers back to one of the plurality of adder units (as being recited at line 5 of claim 1), refers back to the adder unit (as being recited at line 2 of claim 2), or refers back to the "one of said adder units" (as being recited at line 3 of claim 5).

Claims 10-13, 15 and 21:

The terms "said adder units", "one of said adder units" in these claims have the similar problems as in the previous claims 3-5. Applicant is requested to make corrections in the claims to avoid these problems.

Claim 7:

At line 2, what is the purpose of having "a data signal"?

At lines 2-3, the phrase "a data signal comprising a plurality of channels" is not logic. It is not clear how a signal can be comprised of hardware (plurality of channels).

Claim 16:

At line 2, what is the purpose of having "a data signal"?

At lines 2-3, the phrase "a data signal comprising a plurality of channels" is not logic. It is not clear how a signal can be comprised of hardware (plurality of channels).

Claim 24:

At lines 11-14, the phrase "performing a plurality of clocked storage operations on a signal, wherein the signal is conveyed on a ... path between a one of said inputs and said output" is unclear.

It is not clear what important role does the "signal" have? What exactly the "signal" is doing in the signal path?

It is also not clear why the signal path is between only one of said inputs (instead of two of said inputs) since each of the sums is formed by two inputs (as being recited at lines 2-7).

Claim 28:

At line 2, what is the purpose of having "a data signal"?

At lines 2-3, the phrase "a data signal comprising a plurality of channels" is not logic. It is not clear how a signal can be comprised of hardware (plurality of channels).

Claim 29:

At line 3, the term "said sums" is confusing. It is not clear whether the term "said sums" refers to a plurality of sums (as recited at lines 2) or refers to both the first and the second sums (as previously recited in claim 24). This is because there are so many different sums have been recited.

Again, at line 6, the term "said sums" is confusing. It is not clear whether the term "said sums" refers to a plurality of sums (as recited at lines 2) or refers to both the first and the second sums (as previously recited in claim 24).

Claim 30:

At lines 13-16, the phrase "means for performing a plurality of clocked storage operations on a signal, wherein the signal is conveyed on a ... path between a one of said inputs and said output" is unclear.

It is not clear what important role does the "signal" have? What exactly the "signal" is doing in the signal path?

It is also not clear why the signal path is between only one of said inputs (instead of two of said inputs) since each of the sums is formed by two inputs (as being recited at lines 2-8).

Claim 34:

At line 2, what is the purpose of having "a data signal"?

At line 3, the phrase "a data signal comprising a plurality of channels" is not logic. It is not clear how a signal can be comprised of hardware (plurality of channels).

Claim 35:

At line 3, the term "said sums" is confusing. It is not clear whether the term "said sums" refers to a plurality of sums (as recited at lines 2) or refers to both the first and the second sums (as previously recited in claim 30). This is because there are so many different sums have been recited.

Again, at lines 7-8, the term "said sums" is confusing. It is not clear whether the term "said sums" refers to a plurality of sums (as recited at lines 2) or refers to both the first and the second sums (as previously recited in claim 30).

Claims 8-9, 17-23, 25-27 and 31-33:

These claims are rejected because they depend on claims 1, 2, 7, 16, 24 and 30 and contain the same problems of indefiniteness.

3. The following rejections are based on the best understanding of the claimed invention by the examiner in view of the ambiguities that exist in the claims as mentioned above (supra ¶s1-2).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted prior art (APA) (figure 2, ¶s [0008]-[0011]).

Claims 1 and 9-10:

APA discloses the invention substantially as claimed. APA teaches (figure 2) an ACSO unit (200) comprising a compare unit (240). The ACSO unit (200) also comprises two adder units (210 & 220) and a selection unit (230) coupling to each others to form a data path (figure 2).

APA does not explicitly teach the plurality of clocked storage stages. APA, however, suggests channels for sending outputs of the adder units (210 & 220) to inputs of the selection unit (230) (figure 2).

It would have been obvious to one skilled in the art at the time the invention was made to realize that a plurality of registers/latches (clocked storage stages) would have been used for sending outputs of APA's adder units (210 & 220) to the inputs of APA's selectors. One having ordinary skill in the art would be motivated to realize so because using registers/latches to control the synchronization of signals on channels is well-known in the art.

Claims 2 and 4:

APA also teaches an adder unit (260) and a ROM (250) (figure 2).

Claim 3:

APA further teaches a register (270) (figure 2). APA does not explicitly teach the signal path. However, it would have been obvious to one skilled in the art at the time the invention was made to house the combination of APA's compare unit (240), APA's adder unit (260) and APA's register (270) and name such a house as a "signal path". One having ordinary skill in the art would be motivated to realize so because housing APA's comparing unit (240), adder unit (260) and register (270) does not affect any performance of the comparing unit (240), the adder unit (260) and the register (270).

Claims 5-6, 11 and 15:

APA does not explicitly teach that at least one of said clock storage stages are coupled at one of an input to one of said adder units and an output of said adder unit. However, it would have been obvious to one skilled in the art at the time the invention was made to realize that a register/latch could have been used and such an input of the register/latch would have been coupled to the output of one of APA's adder unit (210, 220). One having ordinary skill in the art would be motivated to realize so because using a register/latch to control the synchronization of an output is well-known in the art.

Claims 7-8:

APA discloses plurality of channels (212, 214, 222, 224) for providing inputs into the adder units (210, 220) (figure 2).

Claims 12-13:

APA does not explicitly disclose at least one or a plurality of the clocked storage stages are coupled between the adder unit(s) and the selection unit. APA, however, shows plurality of channels between adder units (210 & 220) and the selection unit (230).

It would have been obvious to one skilled in the art at the time the invention was made to realize that at least one or a plurality of registers/latches (clocked storage stages) would have been used on the channels for sending outputs of APA's adder units (210 & 220) to the inputs of APA's selection unit (230). One having ordinary skill

in the art would be motivated to realize so because using registers/latches to control the synchronization of signals on channels is well-known in the art.

Claim 14:

APA does not explicitly disclose at least one of the clocked storage stages is coupled between the compare unit and the selection unit. APA, however, shows a channel between the compare unit (240) and the selection unit (230).

It would have been obvious to one skilled in the art at the time the invention was made to realize that at least one of registers/latches (clocked storage stages) would have been used on the channels for sending output of APA's compare unit (240) to the inputs of APA's selection unit (230). One having ordinary skill in the art would be motivated to realize so because using a register/latch to control the synchronization of signals on a channel is well-known in the art.

Claims 16, 17 and 19-20:

Claims 16, 17 and (19-20) are rejected for reasons similar to those set forth against claims 7, 8 and 9 respectively.

Claims 18 and 21:

Claims 18, 21 are rejected for reasons similar to those set forth against claims 13 and 5, respectively.

Claims 22-23:

APA discloses (figure 3) a multiple channel architecture (300) comprising plurality of ACS units (310(1) to 310(N)) (figure 3, ¶ [0012]).

Claims 24 and 29:

APA discloses the invention substantially as claimed. APA teaches (figure 2) an ACSO unit (200) comprising two adder units (210 & 220), each of which receives two inputs (212 & 214, 222 & 224) for generating a sum, and a selection unit (230) for selecting either a sum from one of the adder units (210 & 220).

APA does not explicitly teach the feature of performing a plurality of clocked storage stage operations. APA, however, suggests channels for sending outputs of the adder units (210 & 220) to inputs of the selection unit (230) (figure 2).

It would have been obvious to one skilled in the art at the time the invention was made to realize that a plurality of registers/latches (clocked storage stages) would have been used for sending outputs of APA's adder units (210 & 220) to the inputs of APA's selectors. One having ordinary skill in the art would be motivated to realize so because using registers/latches to control the synchronization of signals on channels is well-known in the art.

Claim 25:

APA further teaches a compare unit (240) for comparing the sums of the adder units (210, 220) and for providing control signals to the selection unit (230) (figure 2).

Claim 26:

APA discloses a ROM (250) for storing offsets, one of the offsets from the ROM (250) and a selected sum are inputted into an adder unit (260) for generate a new likelihood value (figure 2, ¶ [0010]).

Claim 27:

APA discloses that the combination of the compare unit (240), the ROM (250), the adder unit (260) and the register (270) for receiving the sums from the adder units (210 & 220) to produce a second output (280).

Claim 28:

APA does not explicitly a plurality of channels with the same number of the clocked storage stages are coupled between the adder unit(s) and the selection unit. APA, however, shows plurality of channels between adder units (210 & 220) and the selection unit (230).

It would have been obvious to one skilled in the art at the time the invention was made to realize that at least one or a plurality of registers/latches (clocked storage stages) would have been used on the channels for sending outputs of APA's adder units (210 & 220) to the inputs of APA's selection unit (230). One having ordinary skill in the art would be motivated to realize so because using registers/latches to control the synchronization of signals on channels is well-known in the art.

Claims 30-35:

Due to the similarity of claims 30-35 to claims 24-29, these claims are also rejected under the same rationale as applied against claims 24-29, respectively.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571) 272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christine T. Tu/
Primary Examiner
Art Unit 2117

March 12, 2009